REMARKS

Claims 1-4 and 6 were examined and reported in the Office Action. Claims 4 and 6 are rejected. Claims 1-3 are allowed. Claims 4 and 6 are amended. Claims 1-4 and 6 remain. Applicant requests reconsideration of the application in view of the following remarks.

I. 35 U.S.C. §102(b)

It is asserted in the Office Action that claims 4 and 6 are rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 4,914,577 issued to Stewart et al ("Stewart"). Applicant respectfully disagrees.

> According to MPEP §2131, "'[a] claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.' (Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987)). 'The identical invention must be shown in as complete detail as is contained in the ... claim.' (Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989)). The elements must be arranged as required by the claim, but this is not an ipsissimis verbis test, i.e., identity of terminology is not required. (In re Bond, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990))."

Applicant's amended claim 4 contains the limitations of

> initializing the tag block in a semiconductor memory device; and performing a data access operation of the semiconductor memory device in response to a physical unit cell address outputted from the tag block sensing a logical cell block address, the physical unit cell address corresponding to N+1 number of unit cell blocks, wherein the initializing the tag block in a semiconductor memory device including: nullifying N+1 number of unit tag tables in the tag block; selecting all of the N+1 number of unit tag tables; and storing each different logical unit cell block information in the N+1 number of unit tag tables, the logical unit cell block information corresponding to N number of unit cell blocks.

Applicant's amended claim 6 contains the limitations of

> [a] method for a refresh operation of a semiconductor memory device including a cell area having N+1 number of unit cell blocks, each including M number of word lines which respectively are coupled to a plurality of unit cells; a tag block having N+1 number of unit tag tables for sensing a logical cell block address to output a physical unit cell address corresponding to N+1 number of unit cell blocks, each having M number of registers for sensing an update of data, comprising: nullifying the N+1 number of unit tag tables; selecting all the N+1 number of unit tag tables; and storing each different logical unit cell block information in the N number of unit tag tables among the N+1 number of unit tag tables, wherein the N number of unit cell blocks are corresponded to the logical cell block address and one unit cell block is added for accessing data with high speed.

Applicant asserts that Stewart does not disclose, teach or suggest a tag block, having N+1 number of unit tag tables, for sensing a logical cell block address included in an inputted row address to output a physical unit cell address corresponding to N+1 number of unit cell blocks. Herein, the logical cell block address corresponds to N number of unit cell blocks, i.e., a specification of a semiconductor memory device receiving the inputted row address, and the physical unit cell address corresponds to N+1 number of unit cell blocks substantially included in the semiconductor memory device for high speed data access. Stewart, however, does not disclose the physical unit cell address and the logic cell block address according to Applicant's claimed invention.

Therefore, since Stewart does not disclose, teach or suggest all of Applicant's amended claims 4 and 6 limitations, Applicant respectfully asserts that a *prima facie* rejection under 35 U.S.C. § 102(b) has not been adequately set forth relative to Stewart. Thus, Applicant's amended claims 4 and 6 are not anticipated by Stewart.

Accordingly, withdrawal of the 35 U.S.C. §102(b) rejections for claims 4 and 6 are respectfully requested.

CONCLUSION

In view of the foregoing, it is believed that all claims now pending, namely 1-4 and 6, patentably define the subject invention over the prior art of record and are in condition for allowance and such action is earnestly solicited at the earliest possible date.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly extension of time fees. If a telephone interview would expedite the prosecution of this Application, the Examiner is invited to contact the undersigned at (310) 207-3800.

Respectfully submitted,

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Dated: January 29, 2007

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CERTIFICATE OF TRANSMISSION

I hereby certify that this correspondence is being submitted electronically via EFS Web on the date shown below to the United States Patent and Trademark Office.

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Jean Svoboda Date: January 29, 2007